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FIG.1 (PRIOR ART)

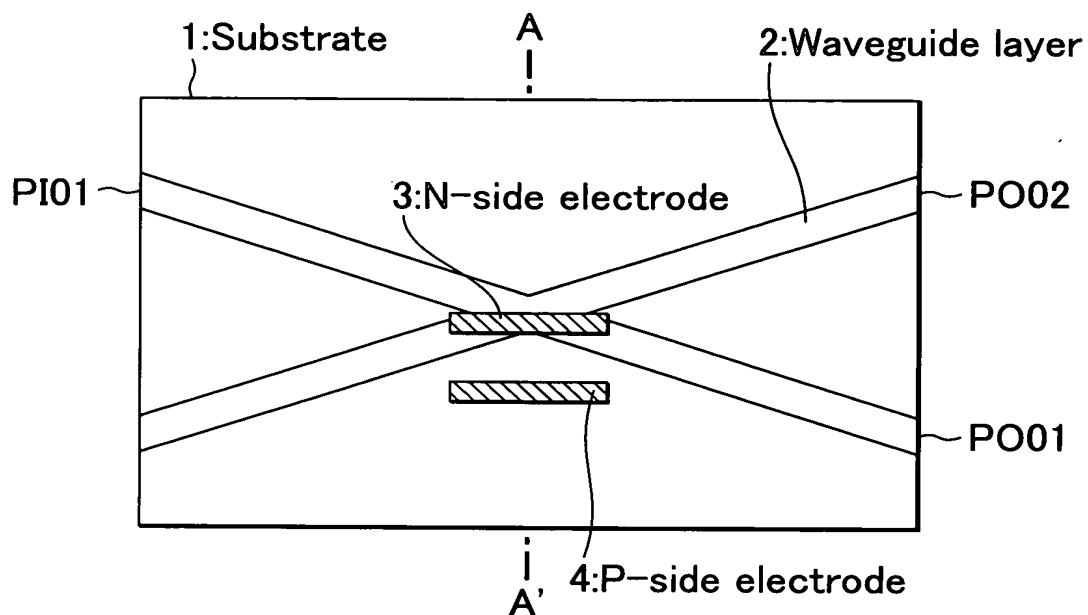


FIG.2 (PRIOR ART)

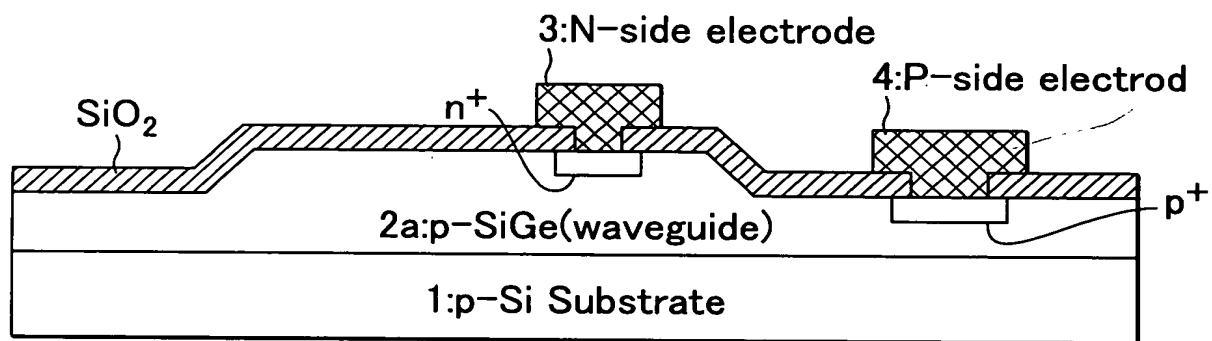


FIG.3 (PRIOR ART)

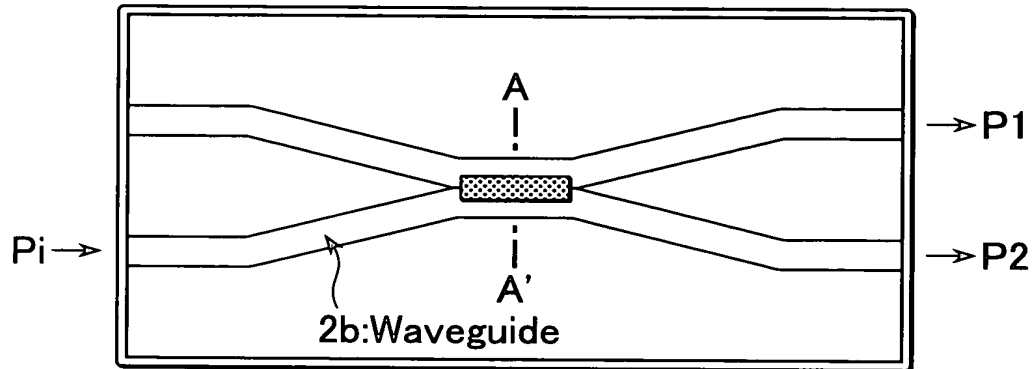


FIG.4 (PRIOR ART)

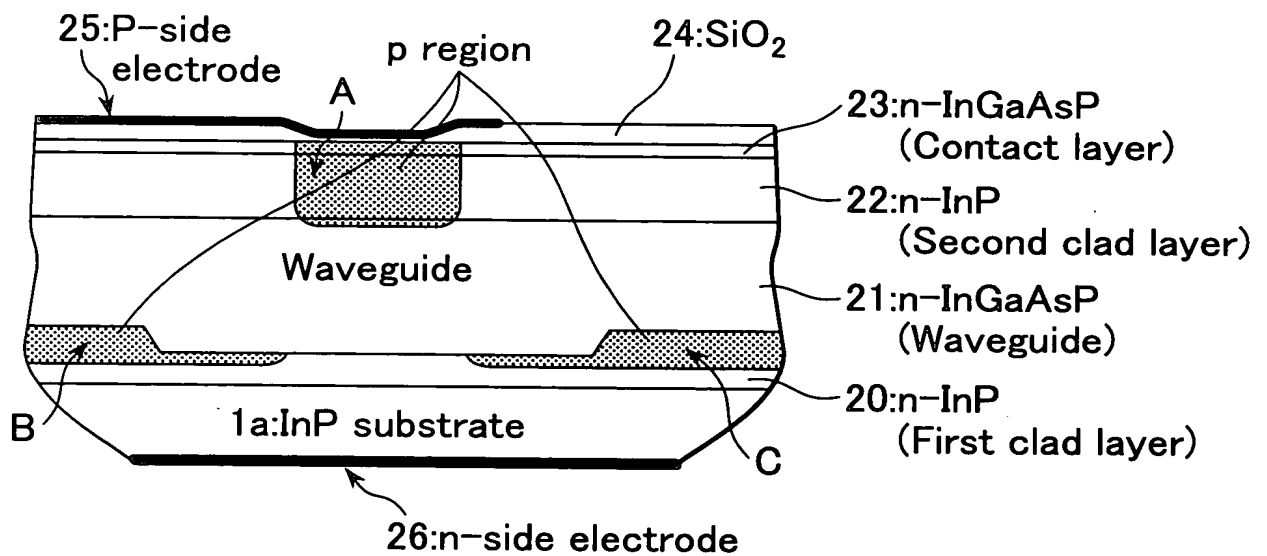


FIG.5

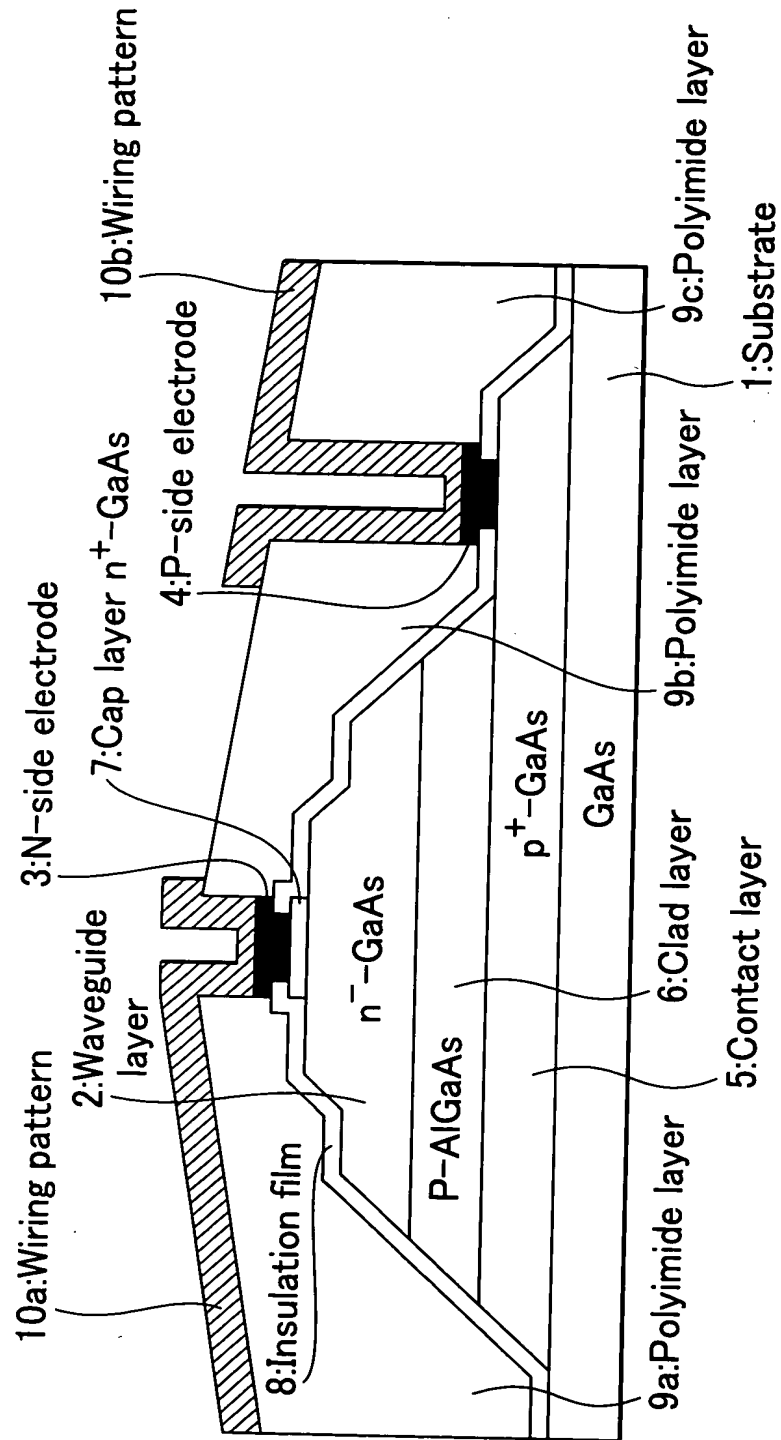


FIG. 6

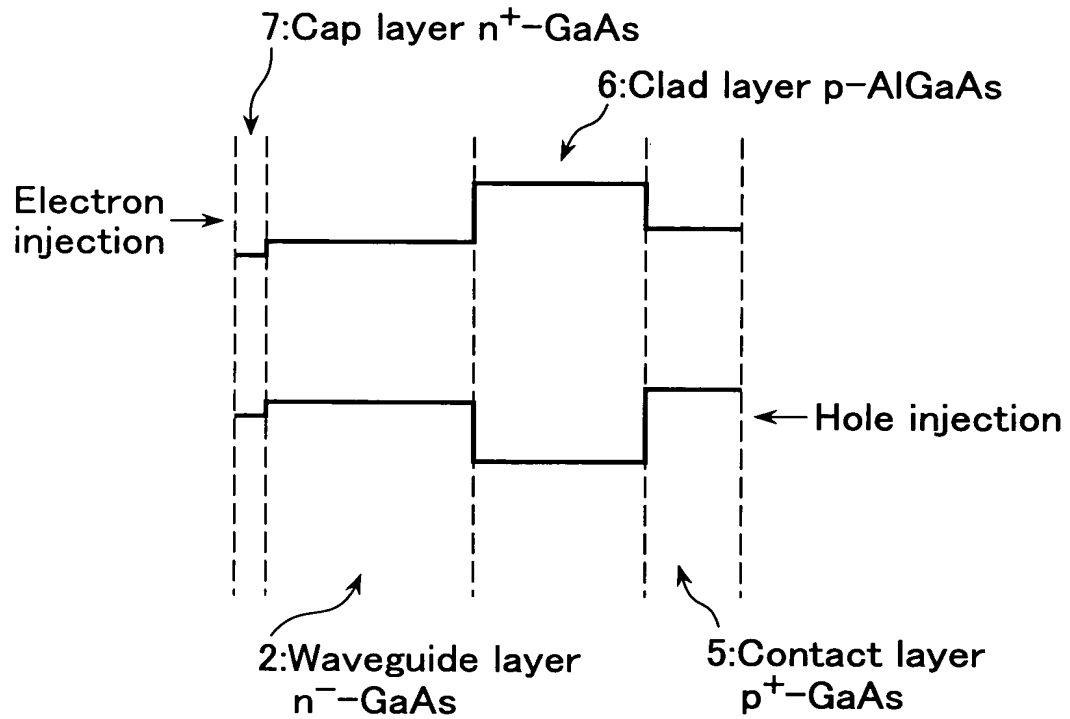
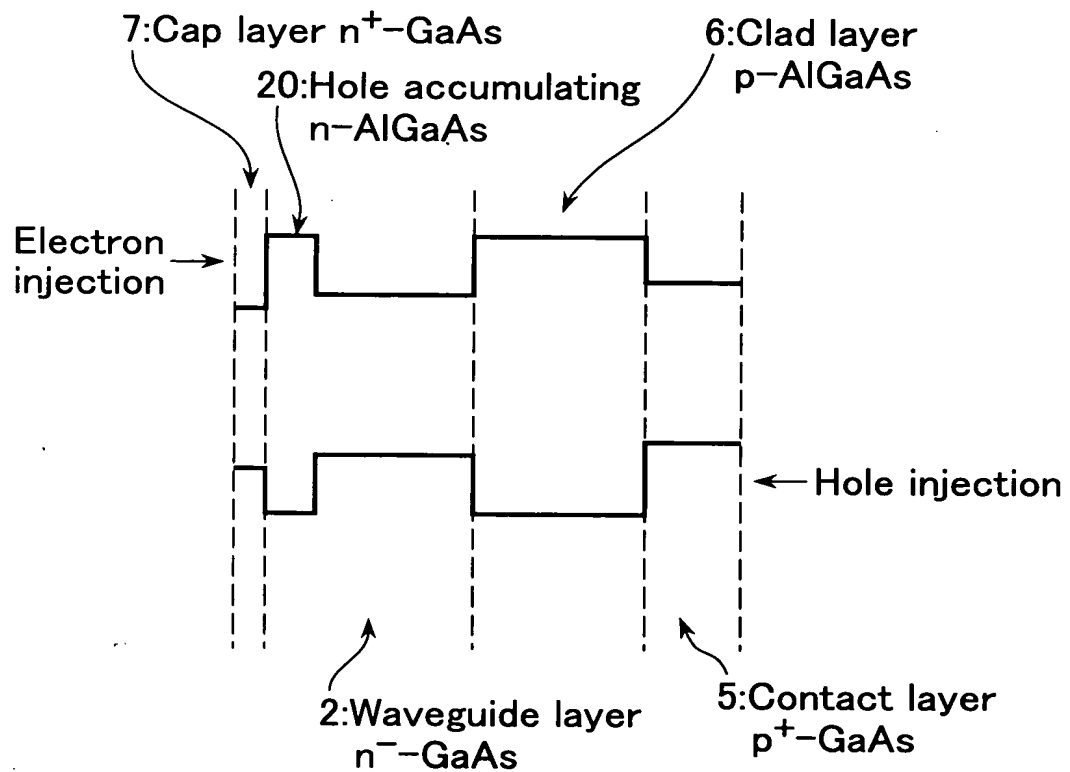


FIG. 7



A cross-sectional diagram of a semiconductor device structure. The structure consists of several layers: a 1a:InP substrate at the bottom, followed by a 20:First clad layer (n-InP), a 21:Core layer (n-InGaAs), a 22:Second clad layer (n-InP), a 23:Contact layer (n-InGaAs), and a 24:Insulation layer (SiO<sub>2</sub>) at the top. A p region is located within the 24:Insulation layer. A 25:P-side electrode is formed on the p region. A 26:N-side electrode is formed on the 1a:InP substrate. A waveguide is formed in the 21:Core layer. A label 'A' points to the p region, 'B' points to the 25:P-side electrode, and 'C' points to the 26:N-side electrode. The label 'Waveguide' is placed in the core layer.

A cross-sectional diagram of a semiconductor device structure. The structure consists of several layers and regions. At the bottom is the **1a:InP substrate**. Above it is the **20:First clad layer (n-InP)**. The next layer is the **21:Core layer (n-InGaAs)**. Above the core layer is the **22:Second clad layer (n-InP)**. The topmost layer is the **24:Insulation layer (SiO<sub>2</sub>)**. A **23:Contact layer (n-InGaAs)** is located between the insulation layer and the second clad layer. A **30:Third clad layer (n-InP)** is located between the first clad layer and the core layer. A **p region** is located in the core layer. A **26:N-side electrode** is located on the bottom surface of the substrate. Labels **A**, **B**, and **C** are used to indicate specific regions or features. **A** points to the core layer. **B** points to the first clad layer. **C** points to the second clad layer. The **InP clad layer** label points to the first clad layer. The **n-InP** label points to the first clad layer.

FIG.10

Index distribution

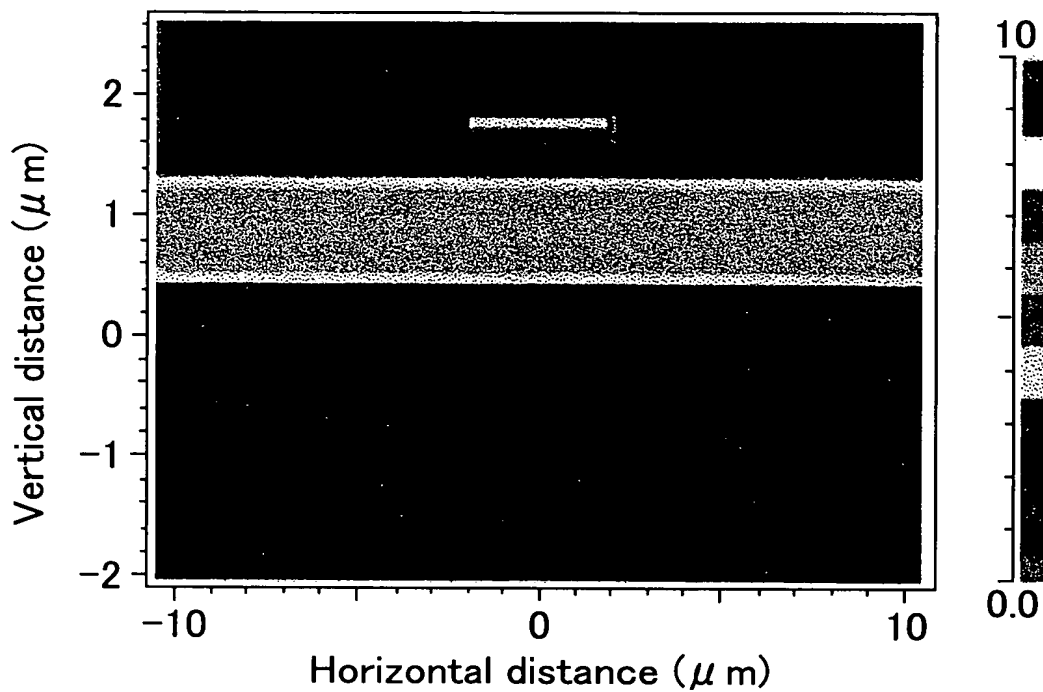


FIG.11

Intensity distribution

